Direct Boost Converter with Zero Voltage Transition and PWM Control (ZVT-PWM)*

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***Summary* – This paper presents the key calculation equations for zero-voltage transition and PWM control in a direct boost converter, and demonstrates results of a converter simulation.**

***Keywords* – direct converter, PWM control, ZVT switching.**

I. INTRODUCTION

ONE BASELINE requirements in engineering of power sources for autonomous power supply systems are enhance,ent of energy conversion efficiency and improvement of the mass and dimensions. As a rule, such systems are based on pulse-type transitro converters with pulse-width control (PWM) and hard switching on the key elements, the latter causing significant dynamic losses and making it impossible to achive high efficiency. Moreover, hard switching is the source of high-noise electromagnetic interference. Reduction of dynamic losses and electromagentic interference can be achieved with the use of transistor converters with PWN and resonant switching (ZVT-PWM) [1, 2, 3]. Such converters are equipped with an additional resonant (switching) circuit that is composed of elements Lr, Cr and an additional transistor switch for soft switching of the main converter switch. Publication [3] discusses PWM converters with resonant switching of the main switch and hard switching of the additional switch. Results of studies show that losses associated with hard switching of the additional switch almost completely negate the advantage offered by reduction of losses due to soft switching of the main switch [3]. Publication [2] presents a diagram of a ZVT-PWM boost converter that implements soft switching for both the main and the additional switches. The publication, however, does not provide the mathematical expressions necessary for analysis of the diagram. Figure 1 shows the diagram of the ZVT-PWM boost converter.

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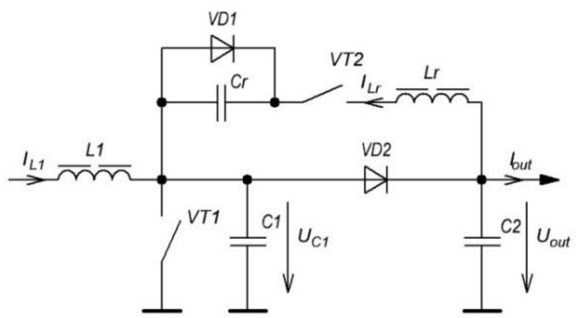

Fig.1. Structural diagram of a converter with zero-voltage transition and PWM control

The converter is a direct boost converter with an additional circuit composed of resonant capacitor C_r, choke coil L_r, diode VD1 and transistor VT2. The distinctive feature of this design solution is that it allows for adjustment of the relative pulse length of the main transistor VT1 when the converter operates in the zero-voltage transition mode, which serves as an advantage of such converter compared to various quasi-resonant design. Figure 2 shows theoretical diagrams of such converter operation.

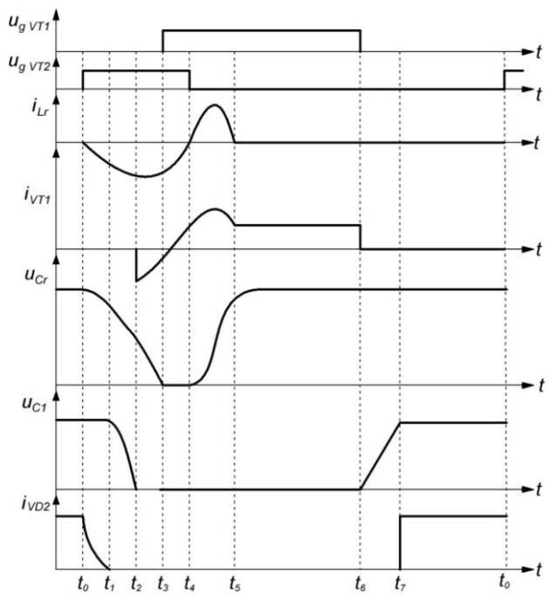

Fig.2. Theoretical diagrams of a converter with zero-voltage transition and PWM control

Figure 2 shows that the transistor switch of VT1 switches in the soft mode: the drain current of the transistor builds up at zero source-drain.

This paper derives formulas for calculation of time interval values for the converter, presents equations for calculation of the resonant circuit, and demonstrates a converter simulation in the MATLAB/Simulink environment.

II. PROBLEM STATEMENT

The objective of this paper is to arrive at analytic expressions allowing to calculate the parameters of a ZVT-PWM converter and to check such expressions by simulating the converter in the MATLAB environment.

III. THEORY

In development of analytic expressions, the following assumptions are made: pulsations of current IL1 and output voltage Uc2 are at level zero; there are no losses in the key elements and diodes; the transition time for transistors and diodes is zero.

We shall divide the operation cycle of the converter into time intervals in which the converter circuit remains unchanged.

A. Time interval $t_0 - t_1$

In this interval, additional transistor VT2 switches on and current builds up in resonant choke coil L_r along the circuit: "$C_r - VT_2 - L_r - VD_2$", as shown in Figure 3.

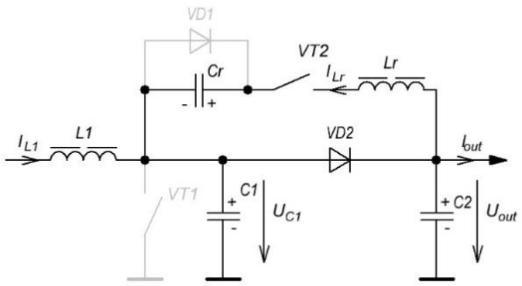

Fig.3. Current flow circuit in interval $t_0 - t_1$

Initial conditions:
Status of semiconductor elements:
VT_1 – closed; VT_2 – open; VD_2 – open; VD_1 – closed.
Initial current and voltage:

$$i_{Lr}(t_0) = 0$$
$$u_{Cr}(t_0) = U_{CrT0}$$
$$u_{C1}(t_0) = U_{out}$$

Variables determining the status of the converter are expressed with the following equations:

$$i_{Lr}(t_{01}) = -\frac{U_{CrT0}}{Z_0} sin(\omega_0 t) \quad (1)$$

$$u_{Cr}(t_{01}) = U_{CrT0} cos(\omega_0 t) \quad (2)$$

$$u_{C1}(t_{01}) = U_{out} \quad (3)$$

where: $\omega_0 = 1 \Big/ \sqrt{L_r \cdot C_r}$ is the angular frequency of the resonant circuit; $Z_0 = \sqrt{L_r / C_r}$ is the characteristic impedance of the resonant circuit.

Time interval Δt_{01} ends when current i_{Lr} reaches the value of. I_{L1}

$$C_2 - L_r - VT_2 - C_r - VT_1 \quad (4)$$

B. Time interval $t_1 - t_2$

In this interval, capacitor C_1 discharges along the circuit: "$C_1 - C_r - VT_2 - L_r - C_2$", as shown in Figure 4.

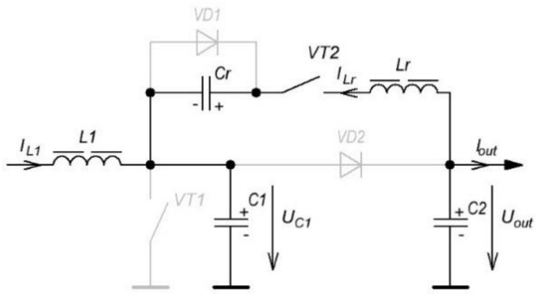

Fig.4. Current flow circuit in interval $t_1 - t_2$

Initial conditions:
Status of semiconductor elements:
VT_1 – closed; VT_2 – open; VD_2 – closed; VD_1 – closed.
Initial current and voltage:

$$i_{Lr}(t_1) = I_{L1},$$
$$u_{Cr}(t_1) = U_{CrT0} cos(\alpha) = U_{CrT1}, \quad (5)$$
$$u_{C1}(t_1) = U_{out}$$

Variables determining the status of the converter are expressed with the following equations:

If the values of C_r and C_1 are comparable, the current of the resonant choke coil is defined with the expression:

$$I_{Lr}(t_{12}) = -I_{L1} cos(\omega_S t) - \frac{U_{CrT1}}{Z_S} sin(\omega_S t) - -I_{L1}\frac{C_S}{C_1}(1 - cos(\omega_S t)) \quad (6)$$

where: $C_S = \frac{C_1 C_r}{C_1 + C_r}$ is the equivalent capacitance of series-connected capacitors C_r and C_1,;

$Z_S = \sqrt{L_r / C_S}$ is the characteristic impedance of the resonant circuit created by series connection of capacitor C_1, capacitor C_r and choke coil L_r.

$\omega_S = 1 \Big/ \sqrt{L_r C_S}$ is the angular frequency of the resonant circuit created by series connection of capacitor C_1, capacitor C_r and choke coil L_r.

If $C_r \ll C_1$, then expression (5) can be simplified as follows

$$i_{Lr}(t_{12}) = -I_{L1} - \frac{U_{CrT1}}{Z_S} sin(\omega_S t) \quad (7)$$

$$u_{Cr}(t_{12}) = -\frac{I_{L1}}{C_r} t + \frac{C_1}{C_r} U_{CrT1}(cos(\omega_S t) - 1) + +U_{CrT1} \quad (8)$$

$$u_{C1}(t_{12}) = U_{CrT1}cos(\omega_S t) - U_{CrT1} + U_{out} \quad (9)$$

Time interval Δt_{12} ends when voltage of capacitor C_1 reaches the value of zero.

$$\Delta t_{12} = \frac{1}{\omega_S} arccos\left(\frac{U_{CrT1} - U_{out}}{U_{CrT1}}\right) = \frac{\beta}{\omega_S} \quad (10)$$

C. Time interval $t_2 - t_3$

In time interval $\boldsymbol{t_2 - t_3}$, resonant capacitor C_r discharges along the circuit: "$C_1 - L_1 - VD_{VT2} - C_r - VT_1$". Figure 5 shows the current flow circuit.

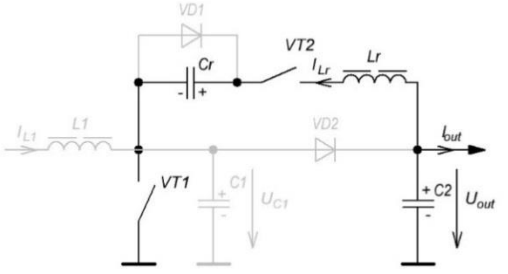

Fig.5. Current flow circuit in interval $t_2 - t_3$

Initial conditions.
Status of semiconductor elements:
VT_1 – open; VT_2 – open; VD_2 – closed; VD_1 – closed.
Initial current and voltage:

$$i_{Lr}(t_2) = -I_{L1} - \frac{U_{CrT1}}{Z_S} sin(\beta) = I_{LrT2}$$

$$u_{Cr}(t_2) = -\frac{I_{L1}}{Cr}\frac{\beta}{\omega_S} + \frac{C_1}{C_r}U_{CrT1}(cos(\beta) - 1) + U_{CrT1} = U_{CrT2}$$

$$u_{C1}(t_2) = 0$$

Variables determining the status of the converter are expressed with the following equations:

$$i_{Lr}(t_{23}) = I_{LrT2}\cos(\omega_0 t) + \frac{U_{out} - U_{CrT2}}{Z_0} sin(\omega_0 t) \quad (11)$$

$$\begin{aligned} u_{Cr}(t_{23}) &= I_{LrT2}Z_0 sin(\omega_0 t) + \\ &+ (U_{out} - U_{CrT2}) \cdot (1 - cos(\omega_0 t)) + U_{CrT2} \end{aligned} \quad (12)$$

$$u_{C1}(t_{23}) = 0 \quad (13)$$

Time interval Δt_{23} ends when the voltage of capacitor C_r reaches the value of zero. By setting the voltage of capacitor C_r equal to zero, at time t_{23}, we obtain the following nonhomogeneous equation (14).

$$asin(x) + bcos(x) = c \quad (14)$$

We shall bring the nonhomogeneous equation to a homogeneous form:

$$\begin{aligned} &(c + b) \cdot sin^2\left(\frac{x}{2}\right) - 2a \cdot sin\left(\frac{x}{2}\right)cos\left(\frac{x}{2}\right) + \\ &+ (c - b) \cdot cos^2\left(\frac{x}{2}\right) = 0 \end{aligned} \quad (15)$$

Next, by substituting variables we solve the quadratic equation (15) for $y = tg\left(\frac{x}{2}\right)$. The time interval is calculated from the equation:

$$\Delta t_{23} = \frac{2}{\omega_S} arctg(y_1) \quad (16)$$

where y_1 is the minimum equation root (15).

At time $t = t_3$, transistor VT_1 opens at zero voltage.

D. Time interval $t_3 - t_4$

In this interval, the current of resonant choke coil L_r reduces almost in a linear fashion along the circuit: "$L_r - C_2 - VT_1 - VD_1 - VT_2$", as shown in Figure 6.

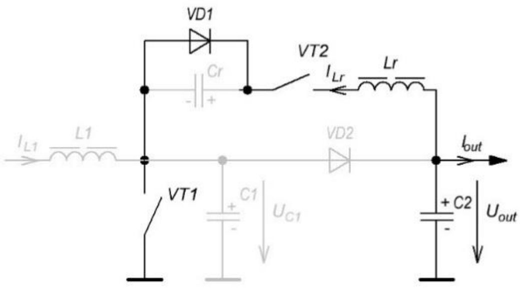

Fig.6. Current flow circuit in interval $t_3 - t_4$

Initial conditions.
Status of semiconductor elements:
VT_1 – open; VT_2 – open; VD_2 – closed; VD_1 – open.
Initial current and voltage:

$$i_{Lr}(t_3) = I_{LrT2}\cos(2y_1) + \frac{U_{out} - U_{CrT2}}{Z_0} sin(2y_1) = I_{LrT3}$$

$$u_{Cr}(t_3) = 0$$

$$u_{C1}(t_3) = 0$$

Variables determining the status of the converter are expressed with the following equations:

$$i_{Lr}(t_{34}) = -I_{LrT3} + \frac{U_{out}}{L_r} \cdot t \quad (17)$$

$$u_{Cr}(t_{34}) = 0 \quad (18)$$

$$u_{C1}(t_{34}) = 0 \quad (19)$$

Time interval Δt_{34} ends when current of choke coil L_r reaches the value of zero.

$$\Delta t_{34} = -\frac{I_{LrT3} \cdot U_{out}}{L_r} \quad (20)$$

At time $t = t_4$, transistor VT_2 switches off at zero current.

E. Time interval $t_4 - t_5$

In time interval $t_4 - t_5$, capacitance C_r receives resonant charge from output capacitor C_2 along the circuit: "$C_2 - L_r - VD_{VT2} - C_r - VT_1$", as shown in Figure 7.

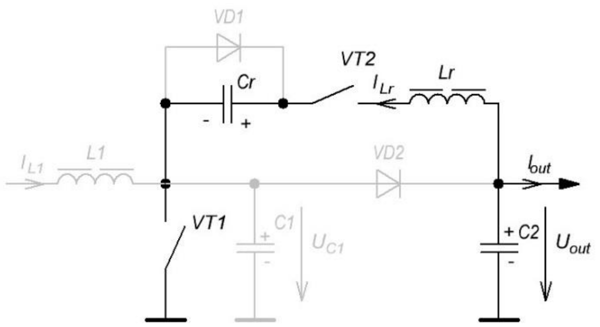

Fig.7. Current flow circuit in interval $t_4 - t_5$

Initial conditions.

Status of semiconductor elements:

VT_1 – open; VT_2 – closed; обратный диод VT_2 – open; VD_2 – closed; VD_1 – closed.

Initial current and voltage:

$$i_{Lr}(t_4) = 0$$
$$u_{Cr}(t_4) = 0$$
$$u_{C1}(t_4) = 0$$
$$u_{C2}(t_4) = U_{out}$$

Variables determining the status of the converter are expressed with the following equations:

При $L_1 - t_2$:

$$i_{Lr}(t_{45}) = \frac{U_{out}}{Z_0} sin(\omega_0 t) \tag{21}$$

$$u_{Cr}(t_{45}) = U_{out}(1 - cos(\omega_0 t)) \tag{22}$$

$$u_{C1}(t_{45}) = 0 \tag{23}$$

Time interval Δt_{45} ends when the current of choke coil L_r reaches the value of zero and the reverse diode of transistor VT_2 switches off. At the same time, capacitor C_r is charged to the double level of output voltage U_{out} and is ready to further switching.

$$\Delta t_{45} = \frac{\pi}{\omega_0} \tag{24}$$

F. Time interval $t_5 - t_6$

In this interval, energy accumulates in choke coil L_1 of the direct converter through the on-transistor VT_1. Figure 8 shows the current flow circuit.

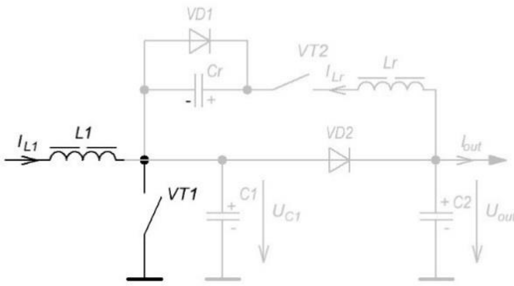

Fig.8. Current flow circuit in interval $t_5 - t_6$

Initial conditions.

Status of semiconductor elements:

VT_1 – open; VT_2 – closed; VD_2 – closed; VD_1 – closed.

Initial current and voltage:

$$i_{Lr}(t_5) = 0$$
$$u_{Cr}(t_5) = 2U_{out}$$
$$u_{C1}(t_5) = 0$$

Duration of the interval is measured with the pulse-width modulator. At moment $t = t_6$, transistor VT_1 switches off at near-zero voltage, because capacitor C_1 is discharged and the growth of its voltage is determined by the intensity of the current of choke coil L_1.

G. Time interval $t_6 - t_7$

In time interval $t_6 - t_7$, voltage builds up in capacitor C_1 along the circuit shown in Figure 9.

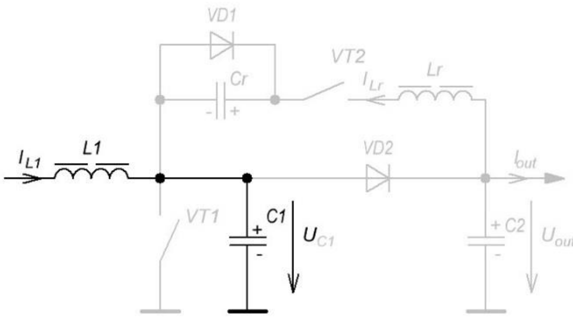

Fig.9. Current flow circuit in interval $t_6 - t_7$

Initial conditions.

Status of semiconductor elements:

VT_1 – closed; VT_2 – closed; VD_2 – closed; VD_1 – closed.

Initial current and voltage:

$$i_{Lr}(t_5) = 0$$
$$u_{Cr}(t_5) = 2U_{out}$$
$$u_{C1}(t_5) = 0$$

Variables determining the status of the converter are expressed with the following equations:

$$i_{Lr}(t_{67}) = 0 \tag{25}$$

$$u_{Cr}(t_{67}) = 2U_{out} \tag{26}$$

$$u_{C1}(t_{67}) = \frac{I_{L1}}{C_1} \cdot t \qquad (27)$$

Time interval Δt_{67} ends when the voltage of capacitor C_1 reaches the value of U_{out} and diode VD_2 is switched on with voltage u_{C1}.

$$\Delta t_{67} = -\frac{I_{LrT3} \cdot L_r}{U_{out}} \qquad (28)$$

H. Time interval $t_7 - t_8$

In time interval $t_7 - t_8$ the energy accumulated in choke coil L_1 is transferred in load through the on-diode VD_2 along the circuit, as shown in Figure 10.

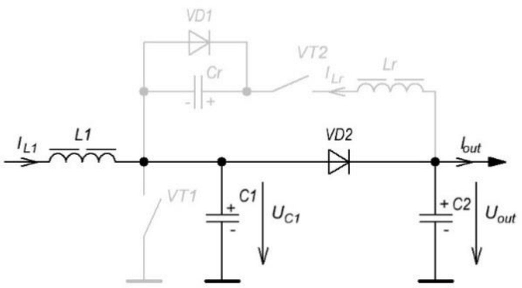

Fig.10. Current flow circuit in interval $t_7 - t_8$

Initial conditions.

Status of semiconductor elements:

VT_1 –closed; VT_2 – closed; VD_2 – open; VD_1 – closed.

Initial current and voltage:

$$i_{Lr}(t_7) = 0 \qquad (29)$$

$$u_{Cr}(t_7) = 2U_{out} = U_{CrT0} \qquad (30)$$

$$u_{C1}(t_7) = U_{out} \qquad (31)$$

Pulse time is measured with the pulse-width modulator. At moment $t = t_8 = t_0$, transistor VT_2 switches on at zero current. Then the process repeats. Expression (30) shows that the voltage of resonant capacitor C_r, at moment t_0, equals $2U_{out}$.

K. Plotting time graphs of switching processes.

Diagrams of the current of resonant choke coil $i_{Lr}(t)$ and voltage of resonant capacitance $u_{Cr}(t)$ are plotted using equations (32) and (33):

$$i_{Lr}(t) = \begin{cases} i_{Lr}(t_{01}), t_0 \le t < t_1 \\ i_{Lr}(t_{12}), t_1 \le t < t_2 \\ i_{Lr}(t_{23}), t_2 \le t < t_3 \\ i_{Lr}(t_{34}), t_3 \le t < t_4 \\ i_{Lr}(t_{45}), t_4 \le t < t_5 \\ 0, t_5 \le t < t_8 \end{cases} \qquad (32)$$

$$u_{Cr}(t) = \begin{cases} u_{Cr}(t_{01}), t_0 \le t < t_1 \\ u_{Cr}(t_{12}), t_1 \le t < t_2 \\ u_{Cr}(t_{23}), t_2 \le t < t_3 \\ 0, t_3 \le t < t_4 \\ u_{Cr}(t_{45}), t_4 \le t < t_5 \\ 2U_{out}, t_5 \le t < t_8 \end{cases} \qquad (33)$$

Diagrams of the current of transistor $i_{VT1}(t)$ and the voltage of transistor $u_{VT1}(t) = u_{C1}(t)$ are plotted using equations (34) and (35):

$$u_{C1}(t) = \begin{cases} U_{out}, t_0 \le t < t_1 \\ u_{C1}(t_{12}), t_1 \le t < t_2 \\ 0, t_2 \le t < t_7 \\ U_{out}, t_7 \le t < t_8 \end{cases} \qquad (34)$$

$$i_{VT1}(t) = \begin{cases} 0, t_0 \le t < t_1 \\ I_{L1} + i_{Lr}(t), t_1 \le t < t_6 \\ 0, t_6 \le t < t_8 \end{cases} \qquad (35)$$

Figure 11 shows diagrams of the drain current of transistor VT_1 (solid line) and the source-drain voltage of transistor VT_1 (dotted line).

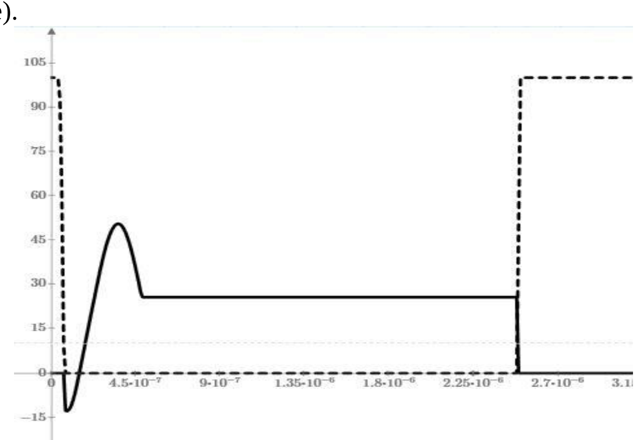

Fig.11. Diagrams of switching processes

Figure 12 shows diagrams of the voltage of resonant capacitor C_r (solid line) and the source-drain voltage of transistor VT_1 (dotted line).

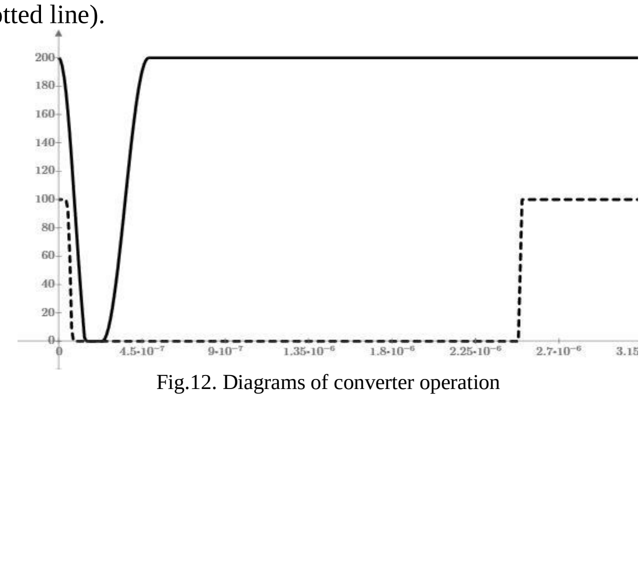

Fig.12. Diagrams of converter operation

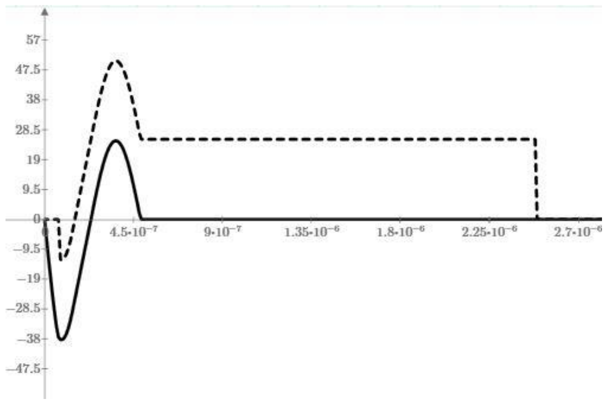

Fig.13. Diagrams of converter operation

Figure 13 shows diagrams of the current of resonant choke coil L_r (solid line) and the drain current of transistor VT_1 (dotted line).

L. Defining the ZVT-PWM computation algorithm

The operating sequence of the converter described above is true of, in time interval $t_1 - t_2$ the voltage of capacitance C_1 reaches the value of zero before the voltage of capacitance. And the higher is the ratio of capacitance C_r value to capacitance C_1 values, the more exact are the expressions (7, 8, 9). Let us assume that the following expression equals zero.

$$C_r \geq 10 \cdot C_1 \quad (36)$$

Assuming that the time of the capacitance C_1 discharge equals a quarter of its natural cycle with angular frequency ω_s, using expression (9) we can calculate that the voltage of capacitance C_r, at moment t_1, should equal U_{out}. Substituting this value of voltage U_{out} in expression (5), we obtain and expression for calculation of Z_0.

$$Z_0 \leq \sqrt{3} \cdot \frac{U_{out}}{I_{L1}} \quad (37)$$

Inductor of the resonant circuit is calculated from expression:

$$L_r = Z_0{}^2 \cdot C_1 \quad (38)$$

As a first approximation, the value of inductor L_1 can be defined for the regular converter with hard switching.

IV. Experimental Results

In order to check the validity of the above expressions, the authors have simulated the ZVT-PWM converter in the MATLAB/Simulink (36)..(38). Figure 14 shows the simulation of the ZVT-PWM converter.

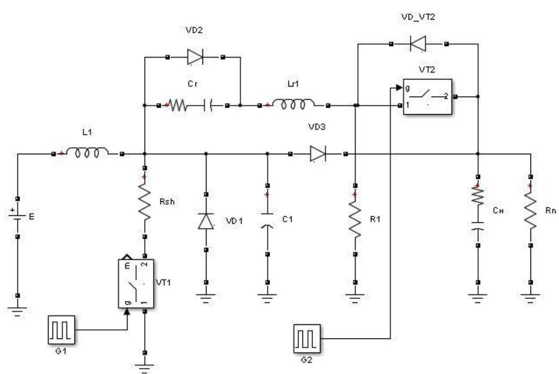

Fig.14. Converter simulation in the MATLAB/Simulink environment

Figue 15 shows the simulation results. The dotted line shows the source-drain voltage of transistor VT1, and the solid line shows the drain current of the transistor.

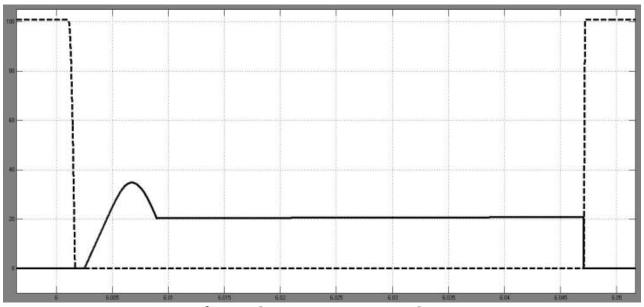

Fig.15. Diagrams of switching processes in the converter transistor

Figure 16 shows diagrams of the current of resonant choke coil Lr (solid line) and the drain current of transistor VT1 (dotted line).

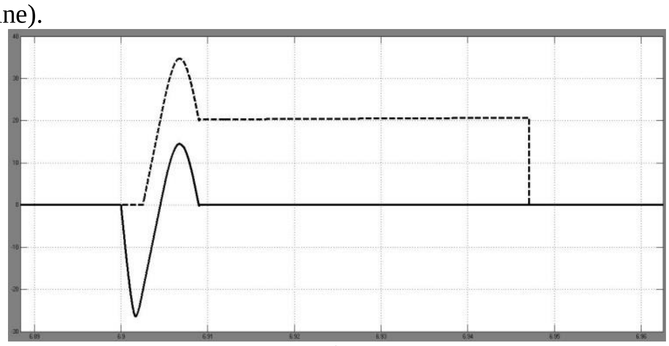

Fig.16. Diagrams of converter operation

Figure 17 shows diagrams of the voltage of resonant capacitor Cr (solid line) and the source-drain voltage of transistor VT1 (dotted line).

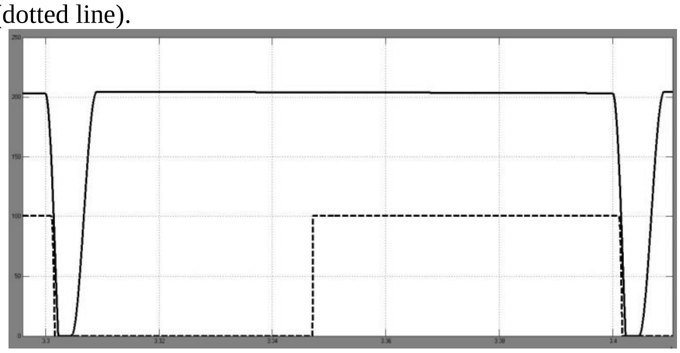

Fig.17. Diagrams of switching processes in the converter transistor

V. Discussion of Results

Analysis of diagrams obtained through calculations and diagrams obtained through simulation of a soft-switching converter in the Simulink environment shows that they are qualitatively identical, which demonstrates the validity of equations obtained analytically and supports their validity for calculation of ZVT-PWM converters.

Graphs plotted during simulation are also identical to the diagrams shown in [2].

VI. Summary and Conclusion

Based on the results obtained by the authors, a conclusion can be made that the described method for reduction of dynamic loss in a converter is valid and implementable.

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